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Target detection circuit implementation for all radar environments

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ABSTRACT

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This paper introduces design and implementation using an FPGA (field programmable gate array) technique of a new method called Maximum Spike Subtraction (MSS) for Constant False Alarm Rate (CFAR) circuit design in radar receivers. The objective of this method is to detect targets accurately in cluttered and multi-interfering target environments. The MSS method depends on selecting the maximum sample amplitude from the input signal sampler and subtracting it from the sum of echo samples in the sliding reference cell window of CFAR. This process provides a more precise estimation of the background noise, which enables the determination of an accurate threshold for target detection. (MSS) the method is evaluated and compared with two significant methods, cell averaged CFAR and ordered statistics (OS)CFAR), to detect targets when multiple targets occur inside a clutter cloud, representing the worst radar environments. The MATLAB clutter test model was used to simulate all of these techniques and apply them to various radar environment instances.

Keywords:
FPGA
Multi targets
Clutter edge
Target detection
Constant False Alarm Rate
CFAR
probability of detection
probability of false alarm

1. INTRODUCTION

The performance of the radar receiver is greatly degraded when there are noise spikes. The goal of the radar receiver is to obtain a constant false alerting rate (CFAR) with the highest possible target detection probability. The echo signal of the targeted target is intercepted by high amplitude signal spikes from interfering targets or undesired echoes (clutter) from the ground, sea, rain, chaff, and other electromagnetic wave reflecting sources. If the false alarm rate has to be reduced, a fixed-threshold detection system cannot be used to detect the targets echo signal from the radar returns in individual range cells since the clutter-plus-noise power is unknown at every given position. Despite the fact that some of these algorithms, such as the greatest of CFAR (GO-CFAR) for clutter cloud problem or ordered statistics (OS-CFAR) algorithms for multi-target environment problems, it required more robust algorithm to deal with the multi-targets inside the clutter cloud situation. dependent on the presence of noise. Receiver has to achieve constant false alarm rate (CFAR) and maximum probability of target detection in order to detect. The signal returns from other electromagnetic reflecting sources referred to as interfering targets or unwanted echoes (clutter) from the ground, sea, rain or chaff and another electromagnetic wave reflecting source that interfere with the echo signal of the desired target. Since the clutter-plus-noise power not known at any given location, a fixed-threshold detection scheme cannot apply to detect the targets echo signal from the radar returns in individual range cells if the false alarm rate is to be controlled. An attractive class of schemes can used to overcome the problem of clutter and to maintain the constant false alarm rate (CFAR) processing schemes that set the threshold adaptively based on local information of total noise power.

Adaptive threshold technique based on the assumption that the probability density function of the noise known except for a few unknown parameters. The surrounding reference cells used to estimate the unknown parameters, and adaptive threshold value will be obtained. From experimental data, the clutter backscattering coefficient (effective echoing area) can be modelled the Rayleigh, exponential, the Weibull distribution or other depending on type of clutter. If the clutter returns are Raleigh envelope distributed, and they assumed identically distributed with the thermal noise, this constitutes the simplest clutter model. Sometimes the environment in which radar operates depends on factors that may yield statistically non-stationary signals with unknown variance at the receiver input. This non- homogeneous environment with clutter edge and non-uniform environments with unwanted multi-interfering targets spikes need robust CFAR algorithm to deal with clutter edge and excise unwanted targets spikes from the background noise estimation to achieve primary wanted targets detection.
Several methods and algorithms used to deal with non-homogeneous and non-uniform environments, Rohling suggested ordered statistics (OS-CFAR) that idea was the beginning of many methods that based on that algorithm [1], such as trimmed mean (TM-CFAR) and censored mean level detector (CMLD-CFAR) [2]. The new solution is to examine, the radar environment before applying suitable CFAR circuit established by applying two or more method on the received signal, and developed solution to use combination of CFAR methods together with selection criteria. to choose appropriate method according to the assumed environment such as variable indexed (VI-CFAR) [3]. Few CFAR algorithms consider the worst radar environments with multi target inside the clutter cloud to happen, therefore it required robust algorithm to deal with this situation. It required very complex algorithm for the worst radar environment that need complex hardware with high processing time or may use two stage-censoring algorithm that make it not suitable for real time applications. All of these algorithms may handle this situation with expense of hardware complexity that expense high processing time that make these algorithms unsuitable for radar real time applications.

2. RESEARCH METHOD

The main objective of this project is to develop a novel CFAR algorithm that can effectively handle clutter edge problems and successfully address the challenges posed by multi-target scenarios. Additionally, the suggested algorithm will be evaluated by creating a MATLAB test model that accurately represents the most unfavorable radar environment. The proposed algorithm will be simulated within the MATLAB environment and applied to the test model. Similarly, other well-known CFAR algorithms will also be simulated and applied to the same test model, allowing for a comparison to determine the algorithm with the best response. Furthermore, the evaluation of these algorithms will consider the processing time required for real-time radar applications. Finally, a mathematical model will be constructed to describe the newly designed algorithm.

2.1 Test Protocol.

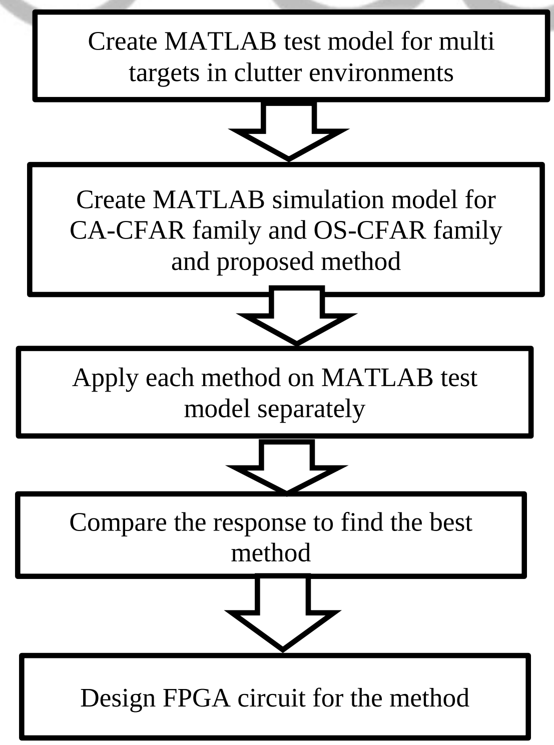

Figure 1 MATLAB testing procedures for proposed method

2.2 The CA-CFAR and OS-CFAR algorithms.

The reference window is constructed from one sample cell obtained from the analog sampler, which converts the radar range echo signal into digital code. Figure 2 displays the CA-CFAR family. The average of the surrounding reference cells is used to estimate the background noise. If the summation of the leading reference window samples is greater than the summation of the lagging reference window samples, the greatest of GO-CFAR is constructed. If the smaller value is selected between them, the smallest of SO-CFAR is constructed. The ordered statistics OS-CFAR algorithm is proposed for multitarget problems and requires prior knowledge of the expected number of targets. The algorithm consists of three steps: sorting the reference cells, estimating the interference power based on the kth sample in the ordered sequence, and choosing the appropriate rank for the OS-CFAR family to function properly. If the sorting process is performed separately for the leading and lagging windows, as shown in figure 3. The greater value between leading and lagging is selected to construct the OSGO-CFAR, while the smaller value is chosen to construct the OSSO-CFAR. [1, 4]

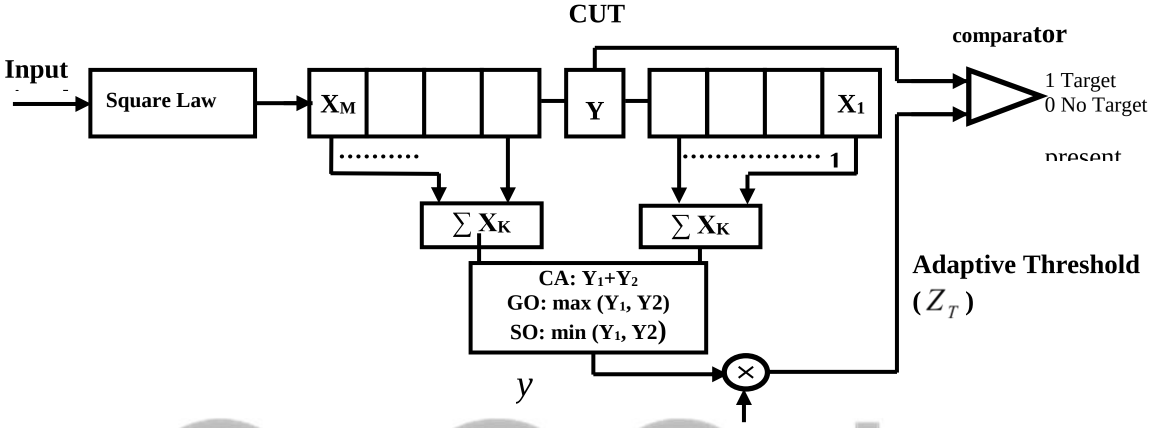

Figure 2 Block diagram of the CA-CFAR family processors.

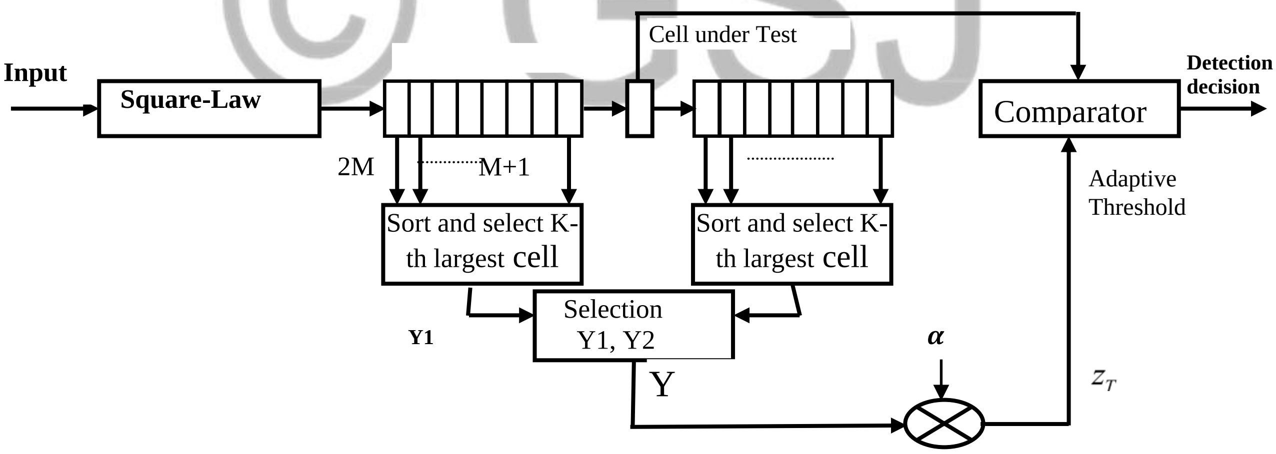

Figure 3 Block diagram of OSGO-CFAR and OSSO-CFAR processors.

2.3 Constructing Maximum Spike Subtraction algorithm.

The principle of this algorithm, Maximum Spike Subtraction MSS--CFAR is to censor the strongest spike from leading reference cells and the strongest from lagging cells by using successive comparison technique that is not used before instead of rank and sort process in order to lessen processing time for radar real time applications that is need time reduction. The new algorithm constructed by three stages:

- The first stage, serial input parallel output shift register is composed of M reference cells, which surround the cell under test located at the shift register centred tap. Range samples are sent serially into shift registers which contain M/2 leading reference cells and M/2 lagging reference cells and the cell under test. This window (M+1) moves along the time duration between two pulses until the entire cell tested.
- The **second stage, is** two parallel processing circuits, the first is two accumulator summing circuits for the leading and the lagging windows. The second circuit is the two maximum sample lock circuits in the leading and the lagging windows. The maximum sample selected from leading and lagging window will be subtracted from the sum of samples in each half of the window.
- The **third stage,** the result averaged and go the selection stage that select either the mean of the leading plus lagging window to construct the Maximum Spike Subtraction MSS-CA-CFAR, or select minimum or maximum of the leading and lagging to construct the Maximum Spike Subtraction smallest of MSS- SO-CFAR and the Maximum Spike Subtraction greatest of GO-CFAR respectively. As shown in the following figure.

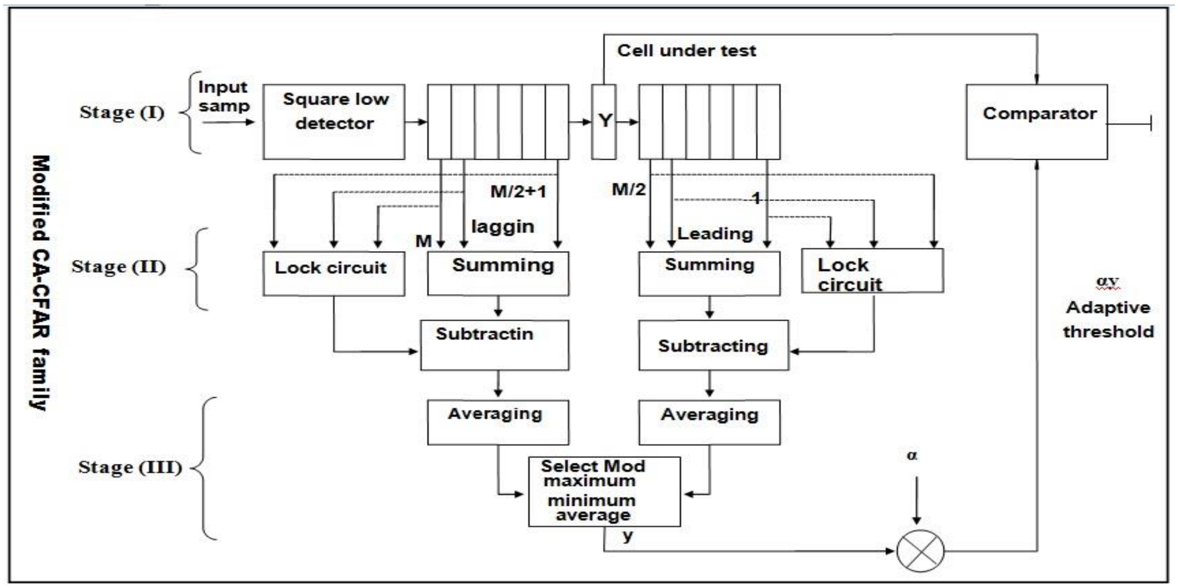

Figure 4 MSS- CA-CFAR family.

2.4 Basic Factors in Simulation Process.

.There are two factors of special importance when dealing with CFAR-algorithms which are the Size of Window (M) and closely separated targets. When M increased, the CFAR loss in a stationary noise background monotonically decreases, together with an increased hardware complexity. Also, with increasing in M an inevitable violation will occur of the inherent assumption that the noise samples are identically distributed over the reference window which is used to estimate the noise in the cell under test. Therefore, in a nonhomogeneous environment CFAR penalty sometimes increases with larger for large M, Also, the likelihood that an interfering target or a 'spiky' clutter return has entered the reference window is obviously larger for larger M [4, 7]. And in closely separated target's situation, another interfering target lies within the reference cells with the primary target (concerned target) the threshold is raised and detection of the primary target is seriously degraded. Sometimes closely separated targets called dense target environment, for example for a radar with a compressed pulse width of 1us (microsecond) and CFAR window with 16-cells on each side of the test cell and if two targets are within one antenna beam width and are separated in range less than 100m the described suppression effect occurs. When clutter cloud appears within reference window the threshold value will rise and the probability of detection degraded, the larger length of clutter cloud (L) means more cell in the clutter cloud [1], and if clutter cloud with high power that give the probability of some small targets to immerse in that cloud. Also, if clutter cloud merged with multi targets the detection problem become more complicated, the worst radar environments when multi targets centered in clutter cloud.

2.5. Weibull probability density function.

CFAR procedures are originally developed using a statistical model of uniform background noise. However, this is not representative of real situations because it is impossible to describe all radar working conditions by

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a single model. For that reason, three different models with clutter clouds and stationary targets are chosen in different critical cases to make comparison between different CFAR procedures at the uniform clutter, clutter edges, and multiple target environments.
The entire 300 echo samples were generated by using MATLAB from Weibull cumulative density function CDF that represented by eq. (2.1).
If x is the amplitude of the output voltage, the Weibull CDF is.

$Q(x) = 1 - e^{(\frac{-x}{b})^{a}}$ ……………………………………………………… (2.1)

The Weibull probability density function PDF (which is the derivative of CDF)

$p(x) = (\frac{a}{b})\left(\frac{x}{b}\right)^{a-1} e^{(\frac{-x}{b})^{a}}$ .... (2.2)

These samples have Weibull PDF at constant skewness (shape) parameter (which is usually taken equal to 2), and it is known from eq. (2.2) that with skewness (shape) parameter equal to 2 the Weibull PDF will take the form of Rayleigh PDF which is used in MATLAB. Therefore, one can use Rayleigh distributed data for calculating multiplier factor to both OS-CFAR and CA-CFAR families.
The targets in these models are assumed to be Marcum targets (non- fluctuation) and the clutter cloud in each model always combines two clutter edges. [3, 20].

2.6. The testing models.

The CFAR algorithm is tested by testing model that constructed from Multi targets that have different magnitudes and to make detection Procedure more complicated from the other models the multi-target are merged with clutter cloud and there is also closely separated targets which are located in different places. For more details there are 20dB at 40^{th} and 50 dB at 50^{th} and 30 dB at 45^{th} and 55^{th} cell positions from 100th to 200th cell clutter cloud which is centered by five closely Targets (2-30dB, 2-40dB, 70dB) respectively, and there is one target 40 dB Magnitude at 230^{th} cell centered between two targets with 20dB magnitude locations 225^{th} and 235^{th} cell respectively, as shown in Figure (5).

The CFAR algorithms deal with four situations, multi target, clutter cloud, multi target merged with clutter, multi-targets located inside clutter. In this model three regions shown: Closely separated multi targets merged with noise, multi targets cantered in clutter cloud representing the worst radar environments.

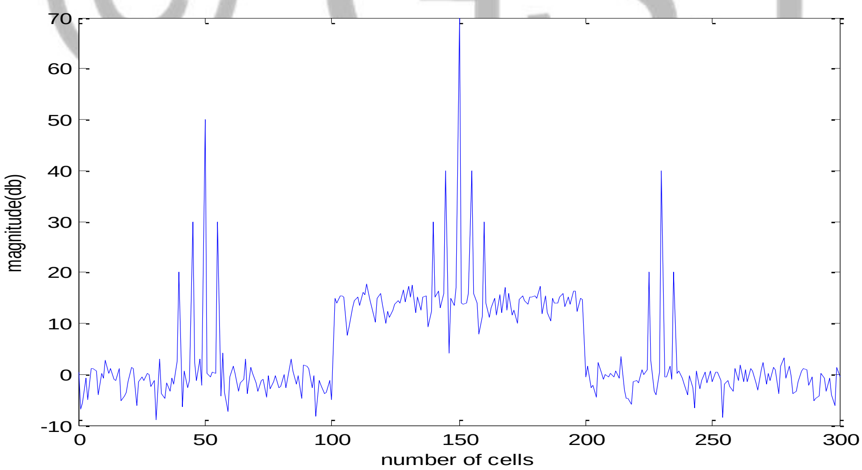

Figure 5 the test model

2.7 applying MATLAB simulated CFAR algorithms.

The response of the CA-CFAR family to the test model as shown in figure (7) and that family contained SO-CFAR and GO-CFAR, Figure (6) shows: GO-CFAR could only detect the strongest target, and fail to detect other targets.CA-CFAR also detects only the strongest target, and fails to detect other targets and also shows bad responses to the clutter edge. SO-CFAR detects all targets, but fall inside the clutter cloud.
OS-CFAR family give better response as shown in Figure (8). The targets are detected successfully, but the leading and falling clutter edge is missed by OSSO-CFAR while OS-CFAR misses only the falling clutter edge. It is shown clearly that OSGO-CFAR detects all the targets and did not affect with the Clutter –edge problem. The output of OSGO-CFAR is larger than OSSO-CFAR and OS-CFAR which means a larger loss in S/N ratio.

On the other hand, from practical circuit design view OSGO-CFAR needs very high processing time and because of sorting process for the samples, it is very hard to implement in an electronic circuit.
The OS-CFAR family takes larger window size (M=48), making the difficulties in background estimation, the only condition for OS-CFAR family to work properly is to choose the rank of the samples which their rank is less than (or equal) the result of subtracting the number of targets from the total number of reference cells, that means the number of the targets must be known to give a good estimation to the background noise.
The response of MSS-CA-CFAR more stable when compare with the other two families since it can detect small targets and detect the two edge of clutter cloud successfully and has the perfect response to noise and less probability of false alarm with less complicated algorithm without sorting process and therefore less processing time and hardware.

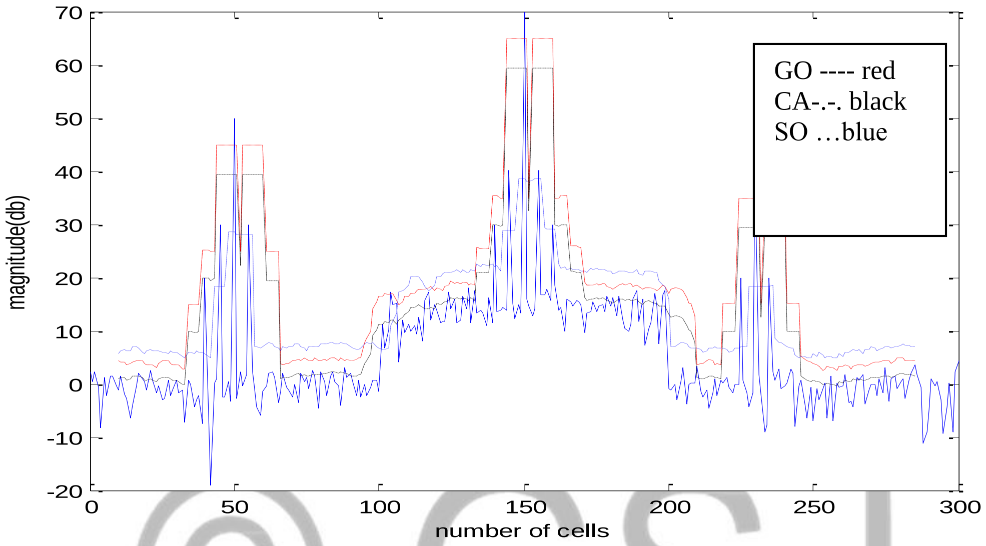

Figure 6. CA-CFAR Family with M=16, P_{fa} $=10^{-6}$ applied to the testing model

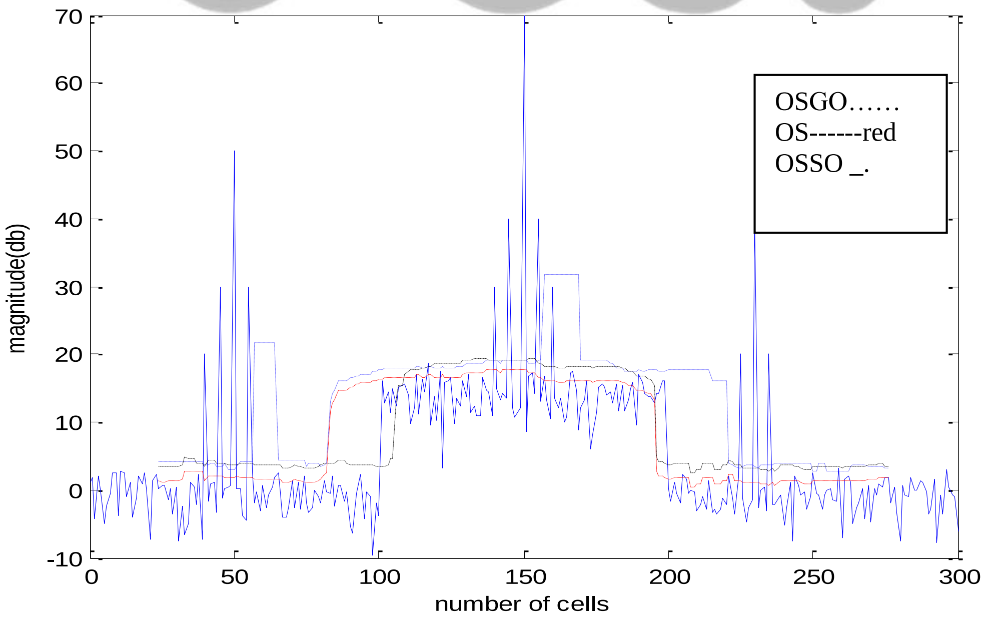

Figure 7. OS –CFAR family applied to test model, M=48, , P_{fa} $=10^{-6}$

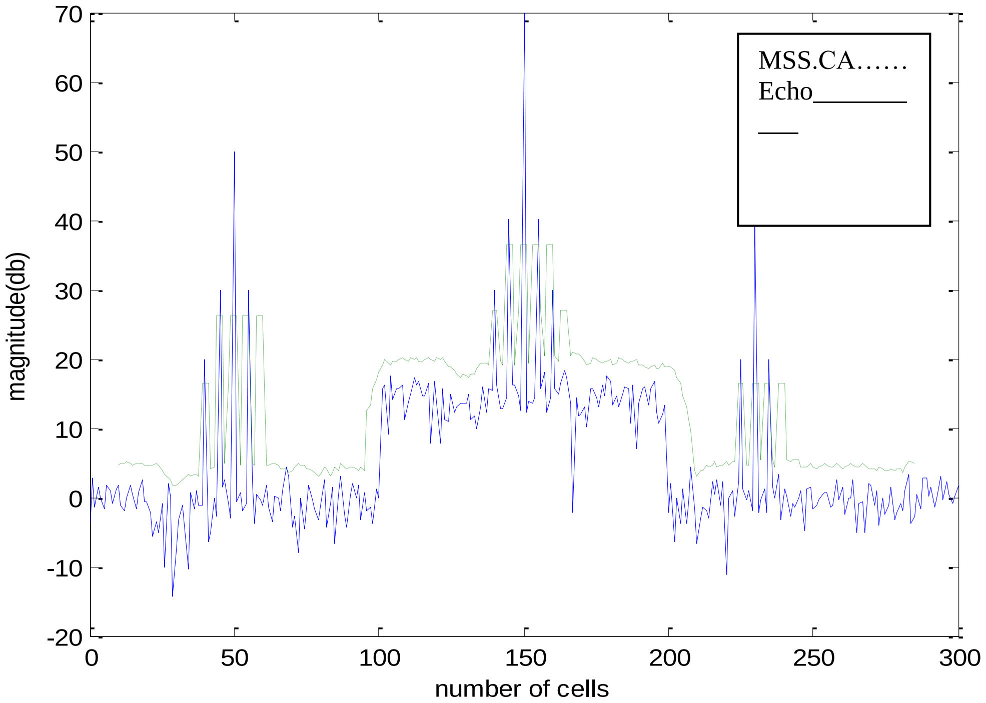

Figure 8. MSS- CA-CFAR response to test model, M=16, $P_{fa} = 10^{-6}$

3. Hardware implementation of MSS-CFAR

Several CFAR algorithms have been proposed in the literature to deal with different radar environments. These different techniques may increase the radar's probability of detection under several environments' conditions, although these methods are advanced from the theoretical aspect of view, they cannot be easily implemented practically, also, they need high computational requirements, which need high processing time, and they need very complex hardware, which may suffer from lack of synchronization and from conflicting signals.

The improvement in the development of the theoretical side of CFAR detection is advanced and very promising, the practical hardware aspect is still beyond the requirements of the high computational signal processing operations. Therefore, few attempts that consider the hardware implementation of CFAR processors have been reported, this problem cannot be solved by technology improvements only, but by using a hardware architecture based on parallel processing. Thus, parallelism is presented in the proposed design in order to speed up the processing time. To design an MSS-CA-CFAR processor circuit using Field-Programmable Gate Array (FPGA) technique to prove that the proposed method can be used successfully in real-time radar applications without any hardware problems, such as conflicting signals or lack of synchronization, and with simple hardware that has suitable processing time.

The field programmable gate array (FPGA) is a programmable digital logic chip that can be programmed to do almost any digital function and it can be reprogrammed to do another function [5]. Most famous Manufacturer of FPGA is The Xilinx Company and Altera Company. The Xilinx Company is the manufacturer of the product of the FPGA family as XC3000, XC4000, XC5200, XC9500, Virtex, and Spartan, which provide wide range devices. MSS- CA-CFAR will be designed using (XC3195a) chip which is a package of 84 pins from XC3000 family. Since it has a sufficient Property to do the job and also sufficient for future improvements.

When designing RADAR CFAR using the XC3000 family with schematic entry, you would typically start by understanding the CFAR algorithm and its requirements. Then, you would translate the algorithm into a circuit diagram using the schematic entry tool provided by the Xilinx design software specific to the XC3000 family.

Considerations for designing RADAR CFAR with schematic entry on the XC3000 family include selecting appropriate components and configuring their properties within the schematic, ensuring proper connectivity and signal flow, and optimizing the design for resource utilization and performance. It is also important to consider the specific constraints of the XC3000 family, such as available logic resources, memory, and timing limitations. Although literature explicitly focusing on using the XC3000 family with schematic entry for RADAR CFAR may be limited, you can refer to general literature on RADAR CFAR algorithms, FPGA design principles, and schematic entry techniques for FPGA designs to gain insights and guidance. Additionally, exploring application notes, tutorials, and reference designs specific to the XC3000 family from Xilinx's documentation and support resources could be helpful. The design steps are as following steps:

1. The samples (as 8-bit digital word) are entered into a circuit that selects maximum sample in each range gate (The analogue to digital converter controlled by the range gate which switched on for the duration of time equal to time interval which is equal to the transmitted pulse width(t).

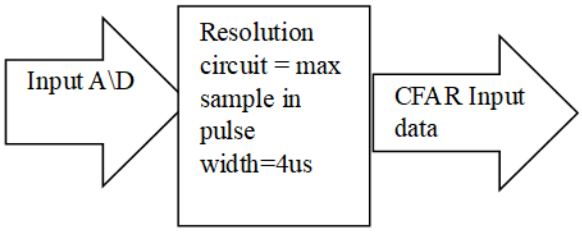

Figure 9 CFAR input.

2. Time base circuit, the base clock signal is used with 8MH (mega-hertz) in analogue to digital converter to sample the signal. This base clock signal is applied to clock dividers to achieve the clock signal needed at every stage of the circuit.
3. The Shifting circuit is serial shift registers that are used to organize cell under test and subtraction process of old cell and addition process of a new cell in order to achieve moving window. Also, this circuit is used to construct leading and lagging window.
4. Two accumulator (more than 8 full adder circuits) are used to add the samples of leading and lagging window.
5. Design of two lock circuits in leading and lagging window respectively that lock on the maximum sample in each window.that the maximum sample subtracted from leading and lagging accumulators.
6. The final stage in the design which selects the average of two windows which applied to multiplier circuit, then to comparator circuit with cell under test to check the target present.

4. Design parameters

There are three design parameters of the radar receiver should be taken into consideration when designing CFAR:

1 Every radar receiver works with certain PRF (pulse repetition frequency) or PRT (pulse repetition time). PRT is the interval between the start of one pulse and the start of another. PRT in this system is chosen to be (304) microsecond (that means low PRF). The PRT of radar system also controls its maximum detectable range by the following formula.

Max range = C.T/2 …………………………. **(4.1)**

C= light speed $=3 \times 10^8$ m/s

m=meter, s =second, T=time period between two successive pulses

Therefore, maximum range =45.6 kilometers.

2 Every radar receiver system transmits a train of pulses and each pulse has a pulse width depending on the work and the purpose of the radar. Pulse width represents the radar resolution. In this system, it is assumed that pulse width=4microsecond= the range gate time interval (t). And receiver resolution=

pulse width, therefore receiver resolution=600 meters and that means that radar could detect targets that are 600meter apart from each other.

3 The base clock frequency=8MH (mega-hertz) that means one sample at 125ns. That means in every (t) there will be (4000/125) =32 samples generated from analogue to digital converter and represented as an 8-bit resolution digital word. The analogue to digital converter controlled by the range gate which switched on for the duration of time equal to (t). Only the max sample is selected from the samples in every (t) since it is more probable to be a target. The CFAR circuit will be reset every pulse repetition period (PRT) and the number of samples that treated with the circuit will be (304/4) =76 sample value in every PRT that will be processed. The sample value represented as an 8-bit resolution digital word.

5. FPGA simulation process

The input value of noise, clutter and targets samples are taken from MATLAB test model, and every cell has one sample taken as maximum sample for range gate duration of 4 microsecond, which represent one cell duration, by taking window size equal 16, after 17 cells (17*4=68 microseconds) the lagging and leading window completed, five targets entered with value equal to (70)decimal and clutter cloud take values of (35,39,41,40,37,36) decimal, the FPGA simulation result as shown in Fig.8. The five-target detection process.

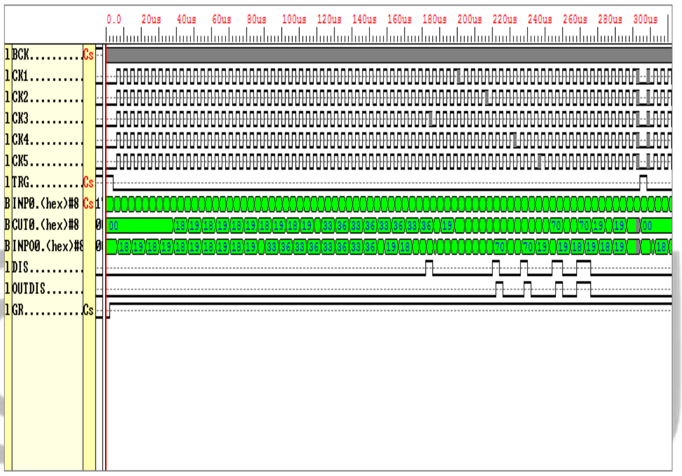

Figure 10. FPGA simulation process.

TABLE I, FPGA implementation report

Design Information Command line	m1map -p xc3195a-09-pc84 -o map.ncd mustafa.ngd mustafa.pcf
Target Device	x3195a
Target Package	pc84
Target Speed	-09
Mapper Version	xc3100a -- D.19
Design Summary	
Number of errors	0
Number of warnings	0
Number of CLBs	259 out of 484 53%
CLB Flip Flops	263
Number of bonded IOBs	11 out of 70 15%
IOB Flip Flops	0
IOB Latches	0
Number of TBUFs	16 out of 1012 1%

6. Result and discussion.

As seen from the simulation result in figure 10 all targets detected by the MSS-CA-CFAR perfectly and also seen from the FPGA implementation report table that the FPGA chip could be improved and updated since there is half of logic blocks still unused, the method implemented easily with no complicated hardware used.

7. CONCLUSION:

The MSS-CA-CFAR, the new algorithm suggested is applied to the testing model as shown in figure (9), the proposed method showed superior response from other method especially in dealing with detecting multi targets centered in clutter cloud. Almost all the CFAR algorithms didn't deal with multi target inside the clutter cloud. They did not propose this worst radar environments to happen, their algorithms yield good performance in clutter edge or multi target, but it required robust algorithm to deal with this situation. The most probable algorithm that may deal with this condition is CFAR method that uses two censoring stage first stages censor interfering targets and the second stage deal with clutter cloud. It assumes that multi target is not centered in clutter cloud so it may handle the problem if multi target merged with clutter (but not inside clutter) and may handle this situation with the expense of hardware complexity that take very high processing time which is unsuitable for radar real time applications. In order to solve the problem of target detection centered in clutter cloud which represent the worst radar environments, the algorithm of MSS-CA-CFAR will improve the performance of the airplane and ship navigation radar system. The algorithm could be used for preventing car collision system and avoid dangerous accidents with the real time CFAR algorithm. The algorithm could be used in the radar systems for highways recognition and limiting vehicle speed.

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